IN THE CLAIMS:

Please amend the claims as set forth below:

1. (Currently Amended) An apparatus comprising:

execution circuitry configured to execute a first instruction which causes an access to first data in a memory;

an error correction code (ECC) check circuit configured to detect an ECC error in response to ~~an~~ the access to the first data ~~in a~~ in the memory; and

a microcode unit coupled to receive an indication that the ECC check circuit has detected the ECC error, wherein the microcode unit, in response to the indication, is configured to dispatch a microcode routine stored by the microcode unit, wherein the microcode routine includes instructions which, when executed, correct the ECC error in the memory;

wherein the microcode unit is coupled to the execution circuitry and the execution circuitry is further configured to execute the instructions in the microcode routine.

2. (Original) The apparatus as recited in claim 1 wherein the ECC check circuit is coupled to receive first ECC data and second ECC data, and wherein the ECC check circuit is configured to detect the ECC error responsive to the first ECC data and the second ECC data, and wherein the first ECC data is generated from the first data in response to storing the first data in the memory, wherein the first ECC data is read in response to the access, and wherein the second ECC data is generated from the first data in response to the access.

3. (Original) The apparatus as recited in claim 2 further comprising an ECC generator coupled to the ECC check circuit and coupled to receive the first data in response to the

access, wherein the ECC generator is configured to generate the second ECC data.

4. (Original) The apparatus as recited in claim 3 further comprising a second memory coupled to the ECC check circuit and to receive an address of the access, wherein the second memory is configured to output the first ECC data in response to the address.

5. (Original) The apparatus as recited in claim 4 wherein the ECC generator is configured to generate third ECC data in response to the instructions in the microcode routine, and wherein the ECC generator is coupled to the second memory, and wherein the second memory is configured to store the third ECC data.

6. (Original) The apparatus as recited in claim 1 further comprising a register coupled to the ECC check circuit, wherein the register is configured to record the ECC error.

7. (Original) The apparatus as recited in claim 6 wherein the register is configured to store an indication of the location of the ECC error in the memory.

8. (Original) The apparatus as recited in claim 7 wherein the indication of the location comprises the address in the memory.

9. (Original) The apparatus as recited in claim 7 wherein the memory comprises a cache, and wherein the indication of the location comprises an index into the cache.

10. (Original) The apparatus as recited in claim 9 wherein the cache is set associative, and wherein the indication of the location further comprises a way in the cache.

11. (Original) The apparatus as recited in claim 9 wherein the cache comprises two or more banks, and wherein the indication of the location further comprises a bank in the cache.

12. (Original) The apparatus as recited in claim 6 wherein the register is further

configured to store an indication of a bit in error within the first data.

13. (Original) The apparatus as recited in claim 6 wherein the register is further configured to store an indication of whether the error is in the first data or in ECC data corresponding to the first data.

14. (Original) The apparatus as recited in claim 6 wherein the microcode routine includes instructions to read the register to identify the ECC error for correction.

15. (Currently Amended) The apparatus as recited in claim 6 wherein the register includes a valid indication indicative of whether or not ~~the register~~ the ECC error ~~recorded in the register~~ is valid in the register.

16. (Original) The apparatus as recited in claim 15 wherein the ECC check circuit is configured to detect a subsequent write to the first data, and wherein the ECC check circuit is configured, if the subsequent write overwrites the ECC error in the first data, to change the valid indication to a state indicating invalid.

17. (Original) The apparatus as recited in claim 16 wherein the microcode routine includes instructions to check the valid indication in the register, and wherein, if the valid indication indicates invalid, the microcode routine is configured to exit without correcting the ECC error.

18. (Original) The apparatus as recited in claim 1 wherein the microcode routine includes instructions to read the first data from the memory, to invert a bit in the first data which is indicated as being in error, and to write the first data back to the memory.

19. (Original) The apparatus as recited in claim 18 further comprising one or more special purpose registers coupled to the memory for providing access to the memory separate from a read/write access path to the memory, and wherein the microcode routine includes instructions to read and write the special purpose registers to correct the ECC

error in the memory.

20. (Original) The apparatus as recited in claim 18 wherein the microcode routine includes load and store instructions for reading and writing the memory to correct the ECC error.

21. (Currently Amended) The apparatus as recited in claim 1 wherein the ECC check circuit~~, if the access is a write which overwrites the ECC error in the memory,~~ is configured to inhibit signaling the ECC error if the access is a write which overwrites the ECC error in the memory.

22. (Original) The apparatus as recited in claim 1 wherein the microcode routine, if the ECC error is uncorrectable, is configured to trap to software.

23. (Currently Amended) A processor comprising:

a microcode unit coupled to receive an indication of an error correction code (ECC) error for first data, wherein the microcode unit, in response to the indication, is configured to dispatch a microcode routine stored by the microcode unit, wherein the microcode routine includes instructions which, when executed, correct the ECC error; and

execution circuitry coupled to receive the instructions from the microcode unit, wherein the execution circuitry is configured to execute the instructions, and wherein the execution circuitry is also configured to execute a first instruction that causes an access to the first data in the memory, wherein the ECC error is detected during the access.

24. (Original) The processor as recited in claim 23 further comprising a register configured to record the ECC error.

25. (Original) The processor as recited in claim 24 wherein the microcode routine includes instructions to read the register to identify the ECC error for correction.

26. (Currently Amended) The processor as recited in claim 25 wherein the register includes a valid indication indicative of whether or not ~~the register~~ the ECC error ~~recorded in the register~~ is valid in the register.

27. (Original) The processor as recited in claim 26 wherein, if the subsequent write overwrites the ECC error in the first data, the valid indication is changed to a state indicating invalid.

28. (Original) The processor as recited in claim 27 wherein the microcode routine includes instructions to check the valid indication in the register, and wherein, if the valid indication indicates invalid, the microcode routine is configured to exit without correcting the ECC error.

29. (Original) The processor as recited in claim 23 wherein the microcode routine includes instructions to read the first data, to invert a bit in the first data which is indicated as being in error, and to write the first data back.

30. (Original) The processor as recited in claim 29 further comprising one or more special purpose registers for providing access to the first data, and wherein the microcode routine includes instructions to read and write the special purpose registers to correct the ECC error.

31. (Original) The processor as recited in claim 29 wherein the microcode routine includes load and store instructions for correcting the ECC error.

32. (Original) The processor as recited in claim 23 wherein the microcode routine, if the ECC error is uncorrectable, is configured to trap to software.

33. (Currently Amended) The processor as recited in claim 23 further comprising a reorder buffer coupled to receive a second indication indicating the ECC error, and wherein the reorder buffer is configured to generate the indication to the microcode unit responsive to retiring the first instruction. ~~an instruction which generated, during execution, the access for which the ECC error is detected.~~

34. (Original) The processor as recited in claim 23 further comprising a cache coupled to the execution circuitry, wherein the cache is configured to store first data and corresponding ECC data, the cache configured to detect an ECC error responsive to an access to the first data in the cache.

35. (Currently Amended) A method comprising:

performing an access to first data in a memory in response to executing a first instruction in execution circuitry;

detecting an ECC error in response to the access; and

dispatching a microcode routine stored by a microcode unit in response to the detecting, wherein the microcode routine includes instructions which, when executed in the execution circuitry, correct the ECC error in the memory.

36. (New) The method as recited in claim 35 further comprising:

recording the ECC error in a register;

detecting a write to the first data subsequent to detecting the ECC error, wherein the write overwrites the ECC error in the first data; and

invalidating the ECC error in the register responsive to detecting the write.

37. (New) The method as recited in claim 36 wherein the microcode routine includes instructions which, when executed, exit without correcting the error if the ECC error in the register has been invalidated.

38. (New) The method as recited in claim 35 further comprising trapping from the microcode routine to software if the ECC error is uncorrectable.

39. (New) The processor as recited in claim 23 further comprising an instruction cache, wherein the first instruction is fetched from the instruction cache for execution by the execution circuitry.

40. (New) A computer system comprising the processor as recited in claim 23 and a peripheral device configured to communicate between the computer system and another computer system.

41. (New) The computer system as recited in claim 40 wherein the peripheral device comprises a modem.

42. (New) The computer system as recited in claim 40 wherein the peripheral device comprises a network interface circuit.

43. (New) The computer system as recited in claim 40 further comprising an audio device.